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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/634,988	08/06/2003	Mitsumi Ito	61282-035	7469

7590 07/14/2006

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EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/634,988	ITO ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 May 2005 and IDS filed 3/5/2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/5/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1, 4-6 13, 15, and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Lavin (US Patent 5,923,563).

2. As for the claims Lavin discloses the invention as claimed, including:

A method and (device) of generating a pattern for a semiconductor device comprising:
A step of designing and arranging a layout pattern of a semiconductor chip [abstract];
A step of extracting an area ratio of the layout pattern [abstract];
A step of determining a most appropriate area ratio of the layout pattern of a layer according to a design rule of the layer, so that the area ratio of the layer can be the most appropriate ratio [abstract];
wherein an area ratio after the completion of forming the dummy pattern is calculated, it is judged whether or not the area ratio is in a range of a predetermined condition, and when the area ratio is not in the range of the predetermined condition [abstract];
a semiconductor device generated by the method of claim 1 and 13 [col. 2, lines 41-44];
a mask pattern for forming a wiring layer, diffusion layer [col. 3, line 66 – col. 4, line 10, and col. 4, lines 49-51];

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 2-3, 7-8, 14, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lavin (US Patent 5,923,563) in view of Smith et al. (US Patent Application Publication 2003/0229875).

4. As for claims 2-3, 7-8, 14, and 17, Lavin discloses the invention substantially as claimed, including the method and device for generating a pattern as disclosed in the rejection of claims 1, 4-6 13, 15, and 18. Lavin further discloses dividing the layout pattern into small regions of a desired size [abstract]; extracting an area ratio for each small region, adding a dummy pattern, preparing a plurality of types of dummy pattern cells, selecting a desired dummy pattern according to the area ratio of the small region [abstract; col. 4];

Lavin does not specifically disclose a gate electrode, and a well [pg. 3, paragraph 0026, see also figs. 7, 9a, 13a, 13c, 16, especially element 34-1, 18, 23, 24, 28; also figs. 1a-b, 2a-b, 5a-b, 6a-b, 11, 14-15, 22a-b, 23, paragraphs 0179, 0186, 0192-0201, 0206, 0215, 0235-0237, 0255, 0259, 0262].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lavin and Smith because both Lavin and Smith are directed towards the design and manufacture of semiconductor devices through the use of dummy patterns, and adding Smith's use of gate electrodes and wells would

allow for the complete manufacture a semiconductor device such as a transistor device [see Smith, abstract].

5. Claims 9-12, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lavin (US Patent 5,923,563) in view of Noble (US Patent Application Publication 2002/0001885).

6. As for the claims, Lavin discloses the invention substantially as claimed, including a method of generating a pattern for a semiconductor as cited in the rejection of claims 1, 4-6, 13, 15, and 18 above. Lavin further discloses an aggregation of dummy patterns of the same or different sizes not to be electrically connected and a dummy pattern including a region overlapped with a dummy pattern on an upper or lower layer of the layer concerned in the vertical direction [col. 4].

Lavin does not specifically disclose that adjusting the layout in the vertical direction for a MOS capacitor cell; and the dummy cell comprising the specific shape as disclosed in claim 12.

Noble discloses a MOS capacitor cell and the configuration of a cell as disclosed in claim 12 [abstract, and figs. 13-24].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Lavin and Noble because adding Noble's MOS cell and cell configuration to Lavin's system would have provided Lavin with the ability to design pattern densities for memory devices such and DRAM that are used widely in integrated circuits for the purpose of storing information.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571)

272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
June 30, 2006